# OV7649FSG Color CMOS VGA (640 x 480) Concept Camera Module

## General Description

The OV7649FSG is a sensor on-board camera and lens module designed for mobile applications where low power consumption and small size are of utmost importance.

Proprietary sensor technology utilizes advanced algorithms to cancel Fixed Pattern Noise (FPN), eliminate smearing, and drastically reduce blooming. All required camera functions are programmable through the serial SCCB interface.

The device can be programmed to provide image output in various fully processed and encoded formats.

The OV7649FSG features the OV7649 CAMERACHIP™. Refer to the *OV7649/OV7149 Datasheet* for chip-specific information.

**Caution: READ THIS FIRST!**
**Prior to finalizing any mechanical or electrical design for production, consult with OmniVision to confirm any final dimensional or electrical pinout data.**

## Features

- 326,688 pixels, VGA/QVGA format, 1/4" lens
- 8 mm x 8 mm x 5.77 module size, flex cable
- Flex cable
- 2.5V operation, low power dissipation
- Serial Camera Control Bus (SCCB) interface
- Function controls:
  - Exposure control
  - Gamma
  - Gain
  - White balance
  - Color matrix
  - Color saturation
  - Hue control
  - Windowing

## Ordering Information

| Product | Package |
|---|---|
| OV07649-FSG | 8 mm x 8 mm x 5.77 mm Flex Cable |

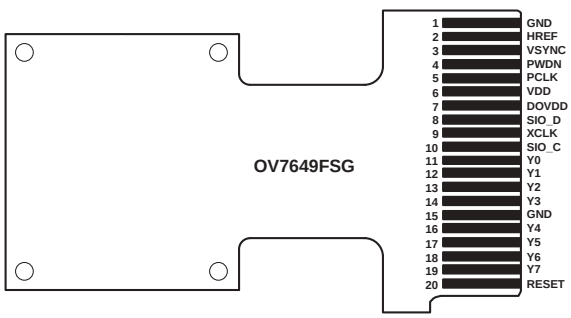
## Applications

- Cell phones
- PDAs
- Picture phones
- Vision toys

## Key Specifications

| | | |
|---|---|---|
| **Array Size** | **VGA** | 640 x 480 |
| | **QVGA** | 320 x 240 |
| **Power Supply** | **Core** | 2.4V to 2.6V DC |
| | **I/O** | 2.25V to 3.6V DC |
| **Power Requirements** | **Active** | 40 mW |
| | **Standby** | 25 µW |
| **Output Formats (8-bit)** | | • YUV/YCbCr 4:2:2 ITU-656<br>• Raw RGB Data |
| **Lens Size** | | 1/4" |
| **Maximum Image Transfer Rate** | **VGA** | 30 fps |
| | **QVGA** | 60 fps |
| **Min. Illumination (3000K)** | **f1.2** | < 1 lux |
| | **f2.8** | < 5 lux |
| **S/N Ratio** | | 46 dB (AGC off, Gamma=1) |
| **Dynamic Range** | | > 48 dB (due to 8-bit ADC limitation)<br>62 db for internal signal |
| **Scan Mode** | | Progressive |
| **Exposure Time** | | 523 to 1 line period (at selected frame rate) |
| **Gamma Correction** | | 0.45/1.0 |
| **Pixel Size** | | 5.6 µm x 5.6 µm |
| **Dark Current** | | 30 mV/s |
| **Fixed Pattern Noise** | | < 0.03% of $V_{PEAK-TO-PEAK}$ |
| **Image Area** | | 3.6 mm x 2.7 mm |
| **Package Dimensions** | | 8 mm x 8 mm x 5.77 mm |

**Figure 1 OV7649FSG Pin Diagram**



## Functional Description

Figure 2 shows the functional block diagram of the OV7649FSG Camera Module. The OV7649FSG includes:

- 1/4" lens
- OV7649 CAMERACHIP image sensor
- Flex cable

**Figure 2 Functional Block Diagram**

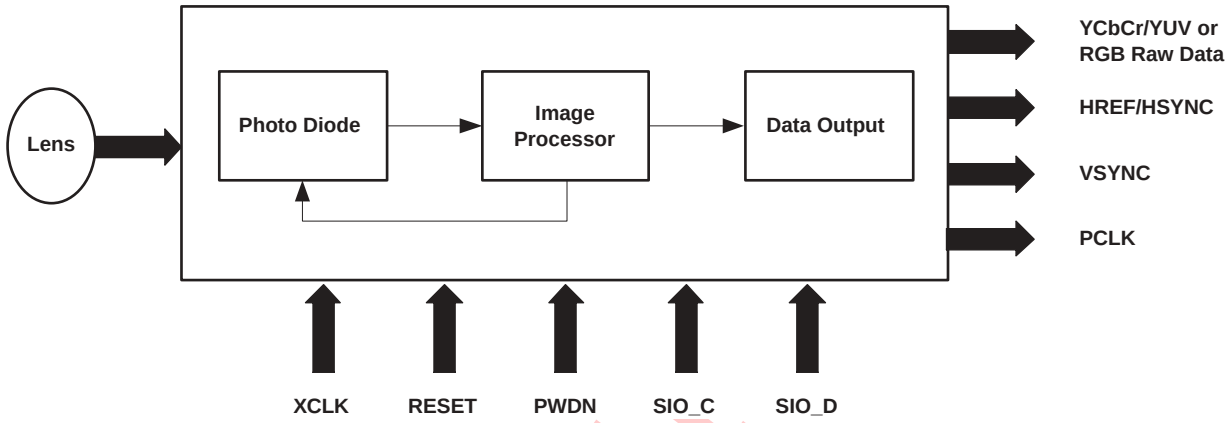
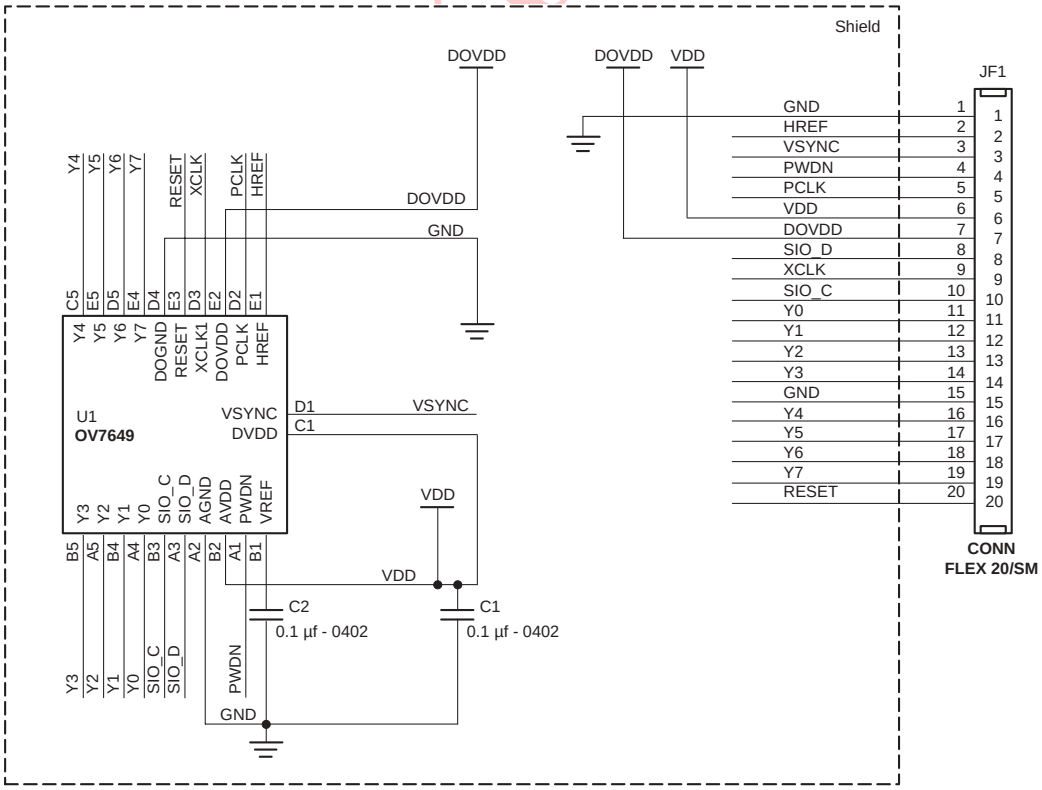



**Figure 3 Module Schematic**




**NOTE:** Connector pin 4 (PWDN) and pin 20 (RESET) should be connected to ground if unused.
VDD is 2.5V sensor analog and digital power.
DOVDD is 2.5V to 3.3V sensor digital I/O power.
C1 should be close to sensor AVDD and AGND.
C2 should be close to sensor VREF and AGND.

## Imaging Specifications

**Table 1 Sensor Image Functions**

| Sensor Imaging Functions | Description |
|---|---|
| Auto Exposure | Module automatically sets correct exposure time. |
| Auto Exposure ON/OFF | Auto exposure can be turned off so the exposure can be set manually. |
| Auto White Balance (AWB) | AWB without companion processor interaction. |
| Auto White Balance OFF | AWB can be turned off. |
| Color Correction | It is possible to adjust for the color filter response of the image sensor as well as for human eye sensitivity. |
| Bayer Pattern Interpolation | (Mosaic or equivalent) The interpolation must be done prior to downsizing the image to avoid artifacts due to incorrect interpolation. |
| Electrical Illumination Flicker Elimination | Interference from 50Hz or 60Hz illumination can be suppressed with manually set frame rate divider. |
| Gamma Correction | Built-in 0.45/1.0 |
| Color Space Conversion | Bayer raw RGB is converted to YCbCr/YUV color space. |
| Image Size Decimation | Size can be altered using the windowing registers. Quarter-format sub-sampling is also provided. |
| Image ON/OFF | Image ON/OFF can be controlled by register settings. |
| Vertical Flip | Transposes the top and bottom sides of the image. |
| Horizontal Flip (Mirror) | Transposes the left and right sides of the image. |
| RGB Output | RGB raw data output available. |
| AGC Gain | Automatic Gain Control (AGC) |
| White Balance | Automatic White Balance |

**NOTE:** OV7649FSG features the OV7649 CAMERACHIP. Refer to the *OV7649/OV7149 Datasheet* for chip-specific information.

**Table 2 Output Specifications**

| Output Image Formats | Description |
|---|---|
| Output Formats | VGA (640 x 480 pixels) |
| | QVGA (320 x 240 pixels) |
| YUV Format | 4:2:2 compliant with CCIR656 |
| YUV Order | YUYV or UYVY |
| Embedded Sync Codes | Sync signals coded in with data output (CCIR656) or output separately. |
| Data Clipping | According to CCIR656 or no clipping. |
| Format in Decimation Mode | PCLK verifies whether or not there is data on every cycle. |

## Pin Description

**Table 3 Pin Description**

| Pin Number | Name | Pin Type | Function/Description |
|---|---|---|---|
| 01 | GND | Power | Shield ground |
| 02 | HREF | Output | HREF output |
| 03 | VSYNC | Output | Vertical sync output |
| 04 | PWDN | Function (default = 0) | Power Down Mode Selection<br>0: Normal mode<br>1: Power down mode |
| 05 | PCLK | Output | Pixel clock output |
| 06 | VDD | Power | Analog and digital power (2.5V) |
| 07 | DOVDD | Power | Digital I/O power (2.5V to 3.3V) |
| 08 | SIO_D | I/O | SCCB serial interface data input and output |
| 09 | XCLK | Input | Clock input |
| 10 | SIO_C | Input | SCCB serial interface clock input |
| 11 | Y0 | Output | Video component output bit[0] |
| 12 | Y1 | Output | Video component output bit[1] |
| 13 | Y2 | Output | Video component output bit[2] |
| 14 | Y3 | Output | Video component output bit[3] |
| 15 | GND | Power | Ground |
| 16 | Y4 | Output | Video component output bit[4] |
| 17 | Y5 | Output | Video component output bit[5] |
| 18 | Y6 | Output | Video component output bit[6] |
| 19 | Y7 | Output | Video component output bit[7] |
| 20 | RESET | Function (default = 0) | Chip reset, with active high. |

# Electrical Characteristics

**Table 4 Operating Conditions**

| Parameter | Min | Max | Unit |
|---|---|---|---|
| Operating temperature (guaranteed performance) | 0 | 40 | °C |
| Operating temperature (chip functional) | -10 | 70 | °C |
| Storage, transportation temperature | -40 | 85 | °C |
| ESD (human body model) | 2000 | | V |

**Table 5 DC Characteristics (0°C < $T_A$ < 70°C, Voltages referenced to GND)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Supply** | | | | | |
| $V_{DD}$ | Supply voltage | 2.4 | 2.5 | 2.6 | V |
| $DOV_{DD}$ | Sensor I/O power | 2.25 | 2.5 | 3.6 | V |
| $I_{DD2}$ | Supply current (2.5V $V_{DD}$, 3.0V $DOV_{DD}$ at 30 fps VGA without digital I/O loading) | | 15 | | mA |
| $I_{DD3}$ | Standby supply current | | 10 | 15 | µA |
| **Digital Inputs** | | | | | |
| $V_{IL}$ | Input voltage LOW | | | 0.8 | V |
| $V_{IH}$ | Input voltage HIGH | 2 | | | V |
| $C_{IN}$ | Input capacitor | | | 10 | pF |
| **Digital Outputs (standard loading 25 pF, 1.2 KΩ to 3 V)** | | | | | |
| $V_{OH}$ | Output voltage HIGH | 2.7 | | | V |
| $V_{OL}$ | Output voltage LOW | | | 0.6 | V |
| **SCCB Inputs** | | | | | |
| $V_{IL}$ | SIO_C and SIO_D ($DOV_{DD}$ = 3V) | -0.5 | 0 | 1 | V |
| $V_{IH}$ | SIO_C and SIO_D ($DOV_{DD}$ = 3V) | 2.5 | 3 | $DOV_{DD}$ + 0.5 | V |

**Table 6 AC Characteristics ($T_A$ = 25°C, $V_{DD}$ = 3V)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **RGB/YCbCr Output** | | | | | |
| $I_{SO}$ | Maximum sourcing current | | 15 | | mA |
| $V_Y$ | DC level at zero signal | | 0.4 | | V |
| | YPP 100% amplitude (without sync) | | 0.7 | | V |
| | Sync amplitude | | 0.4 | | V |
| **ADC Parameters** | | | | | |
| DLE | DC differential linearity error | | 0.5 | | LSB |
| ILE | DC integral linearity error | | 1 | | LSB |

**Table 7 Timing Characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Oscillator and Clock Input** | | | | | |
| $f_{OSC}$ | Frequency (XCLK1) | 10 | 24 | 30 | MHz |
| $t_r$, $t_f$ | Clock input rise/fall time | | | 5 | ns |
| | Clock input duty cycle | 45 | 50 | 55 | % |
| **SCCB Timing (400 Kbps)** | | | | | |
| $t_{BUF}$ | Bus free time between STOP and START | 1.3 | | | µs |
| $t_{HD:SAT}$ | SIO_D change after START status | 0.6 | | | µs |
| $t_{LOW}$ | SIO_D low period | 1.3 | | | µs |
| $t_{HIGH}$ | SIO_D high period | 0.6 | | | µs |
| $t_{HD:DAT}$ | Data hold time | 0 | | | µs |
| $t_{SU:DAT}$ | Data setup time | 0.1 | | | µs |
| $t_{SU:STP}$ | Setup time for STOP status | 0.6 | | | µs |
| **Digital Timing** | | | | | |
| $t_{PCLK}$ | PCLK cycle time | | 41.7 | | ns |
| $t_r$, $t_f$ | PCLK rise/fall time | | | 5 | ns |
| $t_{PDD}$ | PCLK to data valid | | | 5 | ns |
| $t_{PHD}$ | PCLK to HREF delay | 0 | 5 | 10 | ns |

## Timing Specifications

**Figure 4 SCCB Timing Diagram**

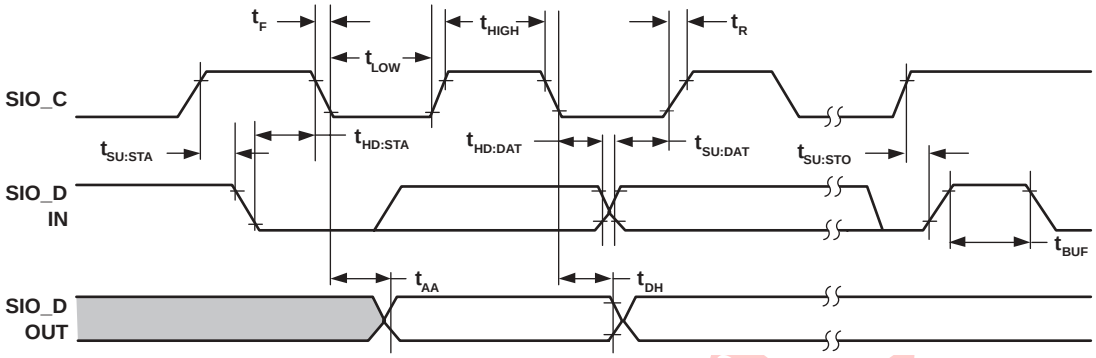
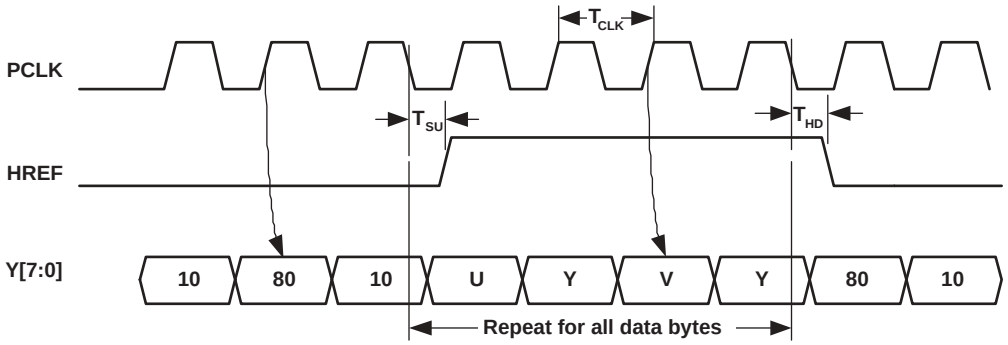


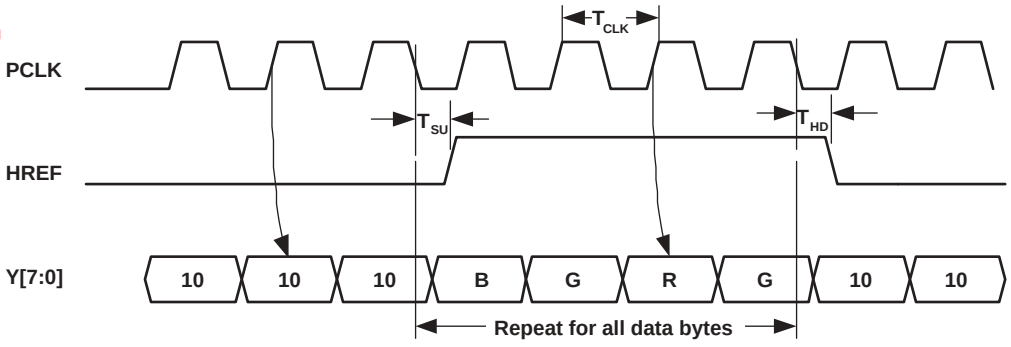

**Figure 5 Pixel Data Bus (YUV Output)**




**Pixel Data 8-bit Timing**
**(PCLK rising edge latches data bus)**

**Note:** $T_{CLK}$ is pixel clock period. $T_{CLK}$ = 41.7ns for 8-bit output if the system clock is 24 MHz.
$T_{SU}$ is the setup time for HREF. The maximum is 10 ns.
$T_{HD}$ is the hold time for HREF. The maximum is 10 ns.

**Figure 6 Pixel Data Bus (RGB Output)**




**Pixel Data 8-bit Timing**
**(PCLK rising edge latches data bus)**

**Note:** $T_{CLK}$ is pixel clock period. $T_{CLK}$ = 41.7ns for 8-bit output if the system clock is 24 MHz.
$T_{SU}$ is the setup time for HREF. The maximum is 10 ns.
$T_{HD}$ is the hold time for HREF. The maximum is 10 ns.

## Register Set

Table 8 shows detailed descriptions of the Device Control registers. The device slave addresses for the OV7649FSG are 42 for write and 43 for read.

**Table 8 SCCB Register List**

| Address (Hex) | Register Name | Default (Hex) | R/W | Description |
|---|---|---|---|---|
| 00 | GAIN | 00 | RW | AGC – Gain control gain setting<br>Bit[7:6]: Reserved<br>Bit[5:0]: Gain control gain setting<br>• Range: [00] to [3F] |
| 01 | BLUE | 80 | RW | AWB – Blue channel gain setting<br>• Range: [00] to [FF] |
| 02 | RED | 80 | RW | AWB – Red channel gain setting<br>• Range: [00] to [FF] |
| 03 | SAT | 84 | RW | Image Format – Color saturation value<br>Bit[7:4]: Saturation value<br>• Range: [0] to [F]<br>Bit[3:0]: Reserved |
| 04 | HUE | 34 | RW | Image Format – Color hue control<br>Bit[7:6]: Reserved<br>Bit[5]: Hue Enable<br>Bit[4:0]: Hue setting |
| 05 | CWF | 3E | RW | AWB – Red/Blue Pre-Amplifier gain setting<br>Bit[7:4]: Red channel pre-amplifier gain setting<br>• Range: [0] to [F]<br>Bit[3:0]: Blue channel pre-amplifier gain setting<br>• Range: [0] to [F] |
| 06 | BRT | 80 | RW | ABC – Brightness setting<br>• Range: [00] to [FF] |
| 07-09 | RSVD | XX | – | Reserved |
| 0A | PID | 76 | R | Product ID number (Read only) |
| 0B | VER | 48 | R | Product version number (Read only) |
| 0C-0F | RSVD | XX | – | Reserved |
| 10 | AECH | 41 | RW | Exposure Value |

**Table 8 SCCB Register List**

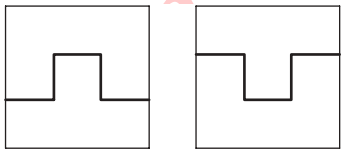
| Address (Hex) | Register Name | Default (Hex) | R/W | Description |
|---|---|---|---|---|
| 11 | CLKRC | 00 | RW | Data Format and Internal Clock<br>Bit[7:6]: Data Format – HSYNC/VSYNC Polarity<br>00: HSYNC = NEG VSYNC = POS<br>01: HSYNC = NEG VSYNC = NEG<br>10: HSYNC = POS VSYNC = POS<br>11: HSYNC = NEG VSYNC = POS<br>  <br>POS NEG<br>Bit[5:0]: Internal Clock Pre-Scalar<br>• Range: [0] to [3F] |
| 12 | COMA | 14 | RW | Common Control A<br>Bit[7]: SCCB – Register Reset<br>0: No change<br>1: Reset all registers to default values<br>Bit[6]: Output Format – Mirror Image Enable<br>Bit[5]: Reserved<br>Bit[4]: Data Format – YUV formatting<br>(when register COMD[0] = 0)<br>0: Y U Y V Y U Y V<br>1: U Y V Y U Y V Y<br>(when register COMD[0] = 1)<br>0: Y V Y U Y V Y U<br>1: V Y U Y V Y U Y<br>Bit[3]: Output Format – Output Channel Select A<br>0: YUV/YCbCr<br>1: RGB/Raw RGB<br>Bit[2]: AWB – Enable<br>Bit[1:0]: Reserved |
| 13 | COMB | A3 | RW | Common Control B<br>Bit[7:5]: Reserved<br>Bit[4]: Data Format – ITU-656 Format Enable<br>0: YUV/YCbCr 4:2:2<br>1: ITU-656 format enabled<br>Bit[3]: Reserved<br>Bit[2]: SCCB – Tri-State Enable – Y[7:0]<br>Bit[1]: AGC – Enable<br>Bit[0]: AEC – Enable |

**Table 8 SCCB Register List**

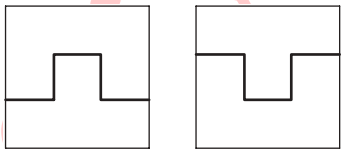
| Address (Hex) | Register Name | Default (Hex) | R/W | Description |
|---|---|---|---|---|
| 14 | COMC | 04 | RW | Common Control C<br>Bit[7:6]: Reserved<br>Bit[5]: Output Format – Resolution<br>0: VGA (640x480)<br>1: QVGA (320x240)<br>Bit[4]: Reserved<br>Bit[3]: Data Format – HREF Polarity<br>0: HREF Positive<br>1: HREF Negative<br>  <br>POS NEG<br>Bit[2:0]: Reserved |
| 15 | COMD | 00 | RW | Common Control D<br>Bit[7]: Data Format – Output Flag Bit Disable<br>0: Frame = 254 data bits (00/FF = Reserved flag bits)<br>1: Frame = 256 data bits<br>Bit[6]: Data Format – Y[7:0]-PCLK Reference Edge<br>0: Y[7:0] data out on PCLK falling edge<br>1: Y[7:0] data out on PCLK rising edge<br>Bit[5:1]: Reserved<br>Bit[0]: Data Format – UV Sequence Exchange<br>(when register COMA[4] = 0)<br>0: Y U Y V Y U Y V<br>1: Y V Y U Y V Y U<br>(when register COMA[4] = 1<br>0: U Y V Y U Y V Y<br>1: V Y U Y V Y U Y |
| 16 | RSVD | XX | – | Reserved |
| 17 | HSTART | 1A | RW | Output Format – Horizontal Frame (HREF Column) Start |
| 18 | HSTOP | BA | RW | Output Format – Horizontal Frame (HREF Column) Stop |
| 19 | VSTRT | 03 | RW | Output Format – Vertical Frame (Row) Start |
| 1A | VSTOP | F3 | RW | Output Format – Vertical Frame (Row) Stop |
| 1B | PSHFT | 00 | RW | Data Format – Pixel Delay Select<br>(Delays timing of the Y[7:0] data relative to HREF in pixel units)<br>• Range: [00] (No delay) to [FF] (256 pixel delay) |
| 1C | MIDH | 7F | R | Manufacturer ID Byte – High (Read only = 0x7F) |
| 1D | MIDL | A2 | R | Manufacturer ID Byte – Low (Read only = 0xA2) |
| 1E | RSVD | XX | – | Reserved |

**Table 8 SCCB Register List**

| Address (Hex) | Register Name | Default (Hex) | R/W | Description |
|---|---|---|---|---|
| 1F | FACT | 01 | RW | Output Format – Format Control<br>Bit[7:5]: Reserved<br>Bit[4]: RGB:565/555 Enable Control<br>0: Disabled<br>1: Enabled<br>Bit[3]: Reserved<br>Bit[2]: RGB:565/555 Mode Select<br>0: RGB:565 output format<br>1: RGB:555 output format<br>Bit[1:0]: Reserved |
| 20 | COME | C0 | RW | Common Control E<br>Bit[7]: Reserved<br>Bit[6]: AEC – Digital Averaging Enable<br>Bit[5]: Reserved<br>Bit[4]: Image Quality – Edge Enhancement Enable<br>Bit[3:1]: Reserved<br>Bit[0]: Y[7:0] 2X $I_{OL}$ / $I_{OH}$ Enable |
| 21-23 | RSVD | XX | – | Reserved |
| 24 | AEW | 10 | RW | AGC/AEC – Stable Operating Region – Upper Limit |
| 25 | AEB | 8A | RW | AGC/AEC – Stable Operating Region – Lower Limit |
| 26 | COMF | A2 | RW | Common Control F<br>Bit[7:3]: Reserved<br>Bit[2]: Data Format – Output Data MSB/LSB Swap Enable (LSB → MSB (Y[7]) and MSB → LSB (Y[0])<br>Bit[1:0]: Reserved |
| 27 | COMG | E2 | RW | Common Control G<br>Bit[7:5]: Reserved<br>Bit[4]: Color Matrix – RGB Crosstalk Compensation Disable (Used to increase each color filter's efficiency)<br>Bit[3:2]: Reserved<br>Bit[1]: Data Format – Output Full Range Enable<br>0: Output Range = [10] to [F0] (224 bits)<br>1: Output Range = [01] to [FE] (254/256 bits)<br>Bit[0]: Reserved |
| 28 | COMH | 20 | RW | Common Control H<br>Bit[7]: Output Format – RGB Output Select<br>0: RGB<br>1: Raw RGB<br>Bit[6]: Device Select<br>0: OV7640<br>1: OV7148<br>Bit[5]: Output Format – Scan Select<br>0: Interlaced<br>1: Progressive<br>Bit[4:0]: Reserved |

**Table 8 SCCB Register List**

| Address (Hex) | Register Name | Default (Hex) | R/W | Description |
|---|---|---|---|---|
| 29 | COMI | 00 | R | Common Control I<br>Bit[7:2]: Reserved<br>Bit[1:0]: Device Version (Read-only) |
| 2A | FRARH | 00 | RW | Output Format – Frame Rate Adjust High<br>Bit[7]: Data Format – Frame Rate Adjust Enable<br>Bit[6:5]: Data Format – Frame Rate Adjust Setting MSB<br>FRA[9:0] = MSB + LSB = FRARH[6:5] + FRARL[7:0]<br>Bit[4]: A/D – UV Channel '2 Pixel Delay' Enable<br>Bit[3:0]: Reserved |
| 2B | FRARL | 00 | RW | Data Format – Frame Rate Adjust Setting LSB<br>FRA[9:0] = MSB + LSB = FRARH[6:5] + FRARL[7:0] |
| 2C | RSVD | XX | – | Reserved |
| 2D | COMJ | 81 | RW | Common Control J<br>Bit[7:3]: Reserved<br>Bit[2]: AEC – Band Filter Enable<br>Bit[1:0]: Reserved |
| 2E-5F | RSVD | XX | – | Reserved |
| 60 | SPCB | 06 | RW | Signal Process Control B<br>Bit[7]: AGC – 1.5x Multiplier (Pre-amplifier) Enable<br>Bit[6:0]: Reserved |
| 61-6B | RSVD | XX | – | Reserved |
| 6C | RMCO | 11 | RW | Color Matrix – RGB Crosstalk Compensation – R Channel |
| 6D | GMCO | 01 | RW | Color Matrix – RGB Crosstalk Compensation – G Channel |
| 6E | BMCO | 06 | RW | Color Matrix – RGB Crosstalk Compensation– B Channel |
| 6F | RSVD | XX | – | Reserved |
| 70 | COMK | 01 | RW | Common Mode Control K<br>Bit[7]: Reserved<br>Bit[6]: Y[7:0] 2X $I_{OL}$ / $I_{OH}$ Enable<br>Bit[5:0]: Reserved |
| 71 | COML | 00 | RW | Common Mode Control L<br>Bit[7]: Reserved<br>Bit[6]: Data Format – PCLK output gated by HREF Enable<br>Bit[5]: Data Format – Output HSYNC on HREF Pin Enable<br>Bit[4]: Reserved<br>Bit[3:2]: Data Format – HSYNC Rising Edge Delay MSB<br>Bit[1:0]: Data Format – HSYNC Falling Edge Delay MSB |
| 72 | HSDYR | 10 | RW | Data Format – HSYNC Rising Edge Delay LSB<br>HSYNCR[9:0] = MSB + LSB = COML[3:2] + HSDYR[7:0]<br>• Range 000 to 762 pixel delays |

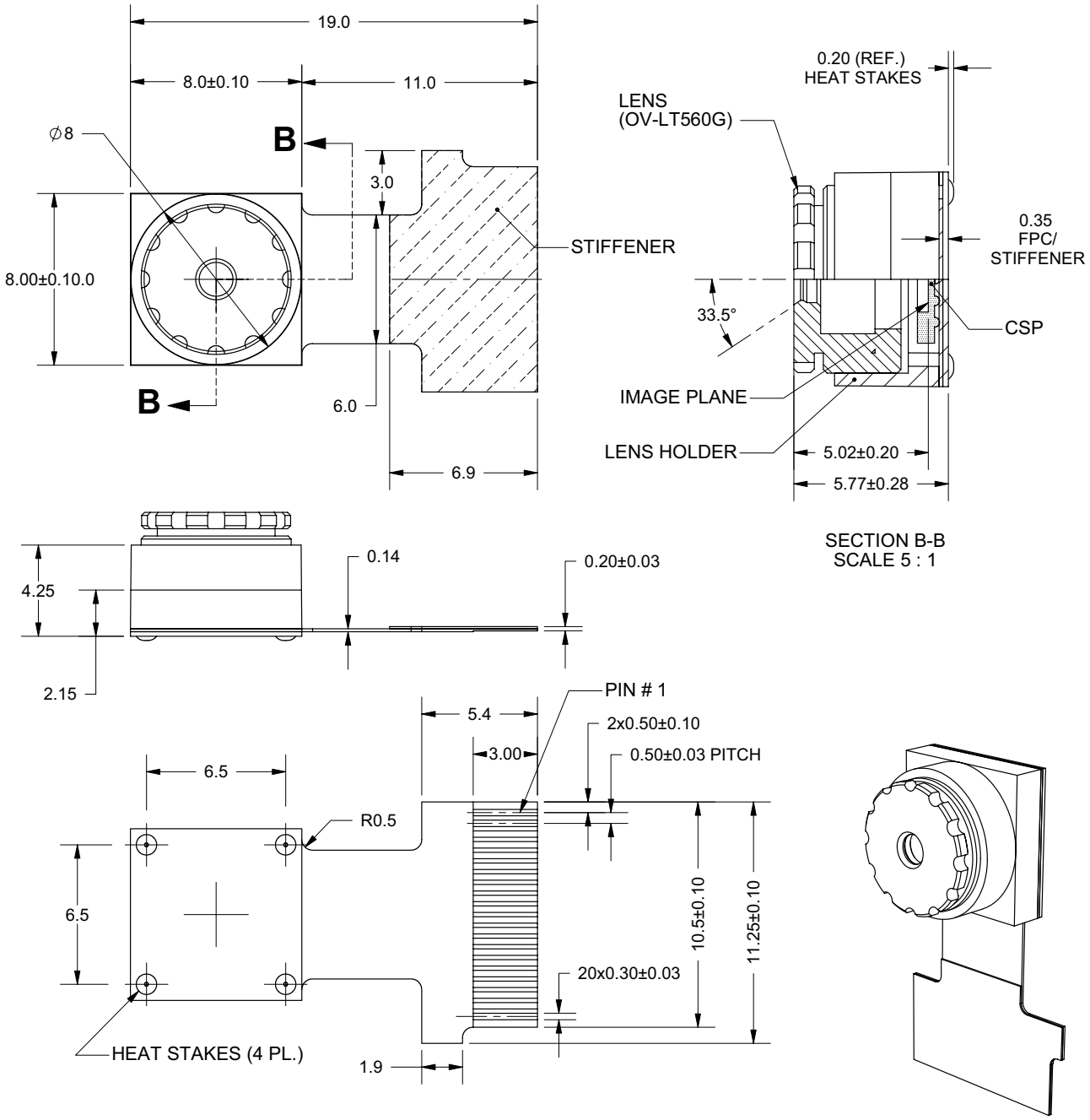
**Table 8 SCCB Register List**

| Address (Hex) | Register Name | Default (Hex) | R/W | Description |
|---|---|---|---|---|
| 73 | HSDYF | 50 | RW | Data Format – HSYNC Falling Edge Delay LSB<br><br>HSYNCF[9:0] = MSB + LSB = COML[1:0] + HSDYF[7:0]<br>• Range 000 to 762 pixel delays |
| 74 | COMM | 20 | RW | Common Mode Control M<br>Bit[7]: Reserved<br>Bit[6:5]: AGC – Maximum Gain Select<br>00: +6 dB<br>01: +12 dB<br>10: +6 dB<br>11: +18 dB<br>Bit[4:0]: Reserved |
| 75 | COMN | 02 | RW | Common Mode Control N<br>Bit[7]: Output Format – Vertical Flip Enable<br>Bit[6:0]: Reserved |
| 76 | COMO | 00 | RW | Common Mode Control O<br>Bit[7:6]: Reserved<br>Bit[5]: Standby Mode Enable<br>Bit[4:0]: Reserved |
| 77-7D | RSVD | XX | – | Reserved |
| 7E | AVGY | 00 | RW | AEC – Digital Y/G Channel Average<br>(Automatically updated by AGC/AEC, user can only read the values) |
| 7F | AVGR | 00 | RW | AEC – Digital R/V Channel Average<br>(Automatically updated by AGC/AEC, user can only read the values) |
| 80 | AVGB | 00 | RW | AEC – Digital B/U Channel Average<br>(Automatically updated by AGC/AEC, user can only read the values) |
| **NOTE:** All other registers are factory-reserved. Please contact OmniVision Technologies for reference register settings. | | | | |

## Package Specifications

Refer to Figure 7 for package information on the OV7649FSG module.

**Figure 7 OV7649FSG Package Specifications**



## Mechanical Specifications

**Table 9 Mechanical Dimensions**

| Parameter | Specification | Comments |
|---|---|---|
| Sensor | 4.95 mm x 4.78 mm | CMOS in housing |
| Lens | Glass/Plastic | |
| Connection Type | 20 x 0.5 mm | Flex cable |
| Housing | 8 mm x 8 mm x 5.77 mm | Excluding mushroom |

## Connector Information

The OV7649FSG uses a 20-pin, 0.5 mm pitch flex cable connector. Table 10 shows a listing of some recommended connectors.

**Table 10 Recommended Connectors**

| Manufacturer | Part No. | Description |
|---|---|---|
| Molex | 52745-2090 | 0.50 pitch FFC/FPC connector |

## Optical Specifications

**Table 11 Optical Specifications**

| Parameter | Specification | Comments |
|---|---|---|
| Lens Elements | Glass/Plastic Hybrid | 3-element (aspheric) fixed focus |
| Viewing Angle | 62.6° diagonal | |
| Focal Length | 3.72 mm | |
| F Number | 2.4 | |
| Focus Range | 30 cm → ∞ | |
| Filter | IR cut | Included |
| Mount Description | M7 x 0.35P | |
| TV Distortion | 1.47% | |
| Focus Adjustment | Fixed | 60 cm |

## Handling Precautions

**WARNING: READ THIS FIRST!**
**Prior to handling any OmniVision flex camera module, read the following precautions.**

- DO NOT try to open the unit enclosure as there is no user-serviceable component inside.
- To prevent damage to the camera module by electrostatic discharge, handle the camera module ONLY after discharging ALL static electricity from yourself and ensuring a static-free environment for the camera module.
- DO NOT touch the top surface of the lens.
- DO NOT press down on the lens.
- DO NOT try to focus the lens.
- DO NOT put the camera module in a dusty environment.
- To reduce the risk of electrical shock and damage to the camera module, turn OFF the power before connect and disconnect the camera module.
- DO NOT bend the flex cable in a sharp angle.
- DO NOT twist the flex cable.
- DO NOT peel the flex cable when you install and uninstall the camera module.
- DO NOT drop the camera module more than 60 cm onto any hard surface.
- To prevent fire or shock hazard, DO NOT expose camera module to rain or moisture.
- DO NOT expose camera module to direct sunlight.
- DO NOT put camera module in a high temperature environment.
- DO NOT use liquid or aerosol cleaners to clean the lens.
- DO NOT make any changes or modifications to camera module.
- DO NOT subject camera module to strong electromagnetic field.
- DO NOT subject the camera module to excessive vibration or shock.

## ***Note:***

- *All information shown herein is current as of the revision and publication date. Please refer to the OmniVision web site (http://www.ovt.com) to obtain the current versions of all documentation.*

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